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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	10/728,172
Filing Date	12-03-2003
First Named Inventor	Gattiker et al.
Art Unit	2825
Examiner Name	GARBOWSKI
Attorney Docket Number	AUS920030654US1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
WP		JONATHAN T-Y CHANG & EDWARD J. McCLUSKEY Quantitative Analysis of Very-Low-Voltage Testing, 1996	
CA		JONATHAN T-Y CHANG, CHAO-WEN TSENG, YI-CHIN, SANJAY WATTAL, MIKE PURTELL AND EDWARD McCLUSKEY Experiemental results for IDDQ and VLV Testing	
RM		R. RODRIGUIZ-MONTANES, J. FIGUERIAS Bridges in Sequential CMOS CIrcuits: Current-Voltage Signature, 1997	
RM		R. RODRIGUIZ-MONTANES, J. FIGUERIAS IDDQ-VDD Signatures for CMOS Circuits with Bridging Defects, 1996	
RM		R. RODRIGUIZ-MONTANES, J. FIGUERIAS Bridges in Sequential CMOS CIrcuits: Current-Voltage Signature, 1997	
WP		ANNE GATTIKER, PHIL NIGH, AND THOMAS VOGELS IC Testing: Background, Directions and Opportunities for Failure Analysis	
HM		HONG HAO AND EDWARD J. McCLUSKEY "Resistive Shorts" within CMOS Gates, 1991	
HM		HONG HAO AND EDWARD J. McCLUSKEY Very-Low-Voltage Testing for Weak CMOS Logic ICs, 1993	
HM		HONG HAO AND EDWARD J. McCLUSKEY Analysis of Gate Oxide Shorts in CMOS Circuits, 1993	
HM		CHARLES F. HAWKINS AND JERRY M. SODEN Electrical Failure Mode Characterization in CMOS ICs	

Examiner Signature		Date Considered	11/2/05

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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WG		JERRY M. SODEN, CHARLES F. HAWKINS & ANTHONY C. MILLER Identifying defects in deep-submicron CMOS ICs, 1996	
WG		JERRY M. SODEN, CHARLES F. HAWKINS, RONALD R. FRITZEMEIER & LUTHER K. HORNING Quiescent Power Supply Current Measurement for CMOs IC Defect Detection, 1989	
WG		DOUG JOSEPHSON, MARK STOREY, DAN DIXON, HEWLETT-PACKARD Microprocessor IDDQ Testing: A Case Study, 1995	
WG		ALI KESHAVARZI, KAUSHIK ROY, MANOJ SACHDEV, CHARLES F. HAWKINS, K. SOUMYANATH, VLVEK DE Multiple-Parameter CMOS IC Testing with Increased Sensitivity for IDDQ, 2000	
WG		BRAM KRUSEMAN, STEFAN van den OETELAAR, AND JOSEP RIUS Comparisons of IDDQ Testing and Very-Low Voltage Testing, 2002	
WG		BORIS LISENKER AND YURI MITNICK Fault Model for VLSI Circuits Reliability Assessment, 1999	
WG		BORIS LISENKER, DMITRY VEINGER AND YURI MITNICK Short High Voltage Stress for Design-to-Process Characterization, 1999	
WG		PHIL NIGH AND ANNE GATTIKER Test Method Evaluation Experiments & Data, 2000	
WG		PHIL NIGH, DAVE VALLETT, ATUL PATEL & JASON WRIGHT Failure Analysis of Timing and IDDQ-only Failures from the SEMATECH Test Methods Experiment, 1998	
WG		ALAN W. RIGHTER, CHARLES F. HAWKINS, JERRY M. SODEN, PETER MAXWELL CMOS IC Reliability Indicators and Burn-In Economics, 1998	

Examiner Signature		Date Considered	11/27/05

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WP		R. RODRIGUIZ-MONTANES, J.A. SEGURA, V.H.CHAMPAC, J. FIGUERAS, J.A. RUBIO Current vs. Logic Testing of Gate Oxide Short, Floating Gate and Bridging Failures in CMOS, 1991	
WD		MICHAEL RUBIN, DAVID LEARY AND SAUL NATAN Yield Enhancement and Yield Management of Silicon Foundries Using IDDQ " Stress Current Signature", 2001	
WP		YASUO SATO, MASAKI KOHNO, TOSHIO IKEDA, IWAO YAMAZAKI, & MASATO HAMAMOTO An Evalution of Defect-Oriented Test: WELL-controlled Low Voltage Test, 2001 IEEE.	
WD		CHAO-WEN TSENG, RAY CHEN, PHIL NIGH & EDWARD J. McCLUSKEY MINVDD Testing for Weak CMOS ICs, 2001 IEEE.	
WD		T.J. VOGELS Effectiveness of I-V Testing in Comparison to IDDQ Tests, 2003 IEEE.	

Examiner Signature		Date Considered	11/2/5

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